NASA Electronic Parts and Packaging (NEPP) Program – Radiation Activities

Kenneth A. LaBel
ken.label@nasa.gov
301-286-9936

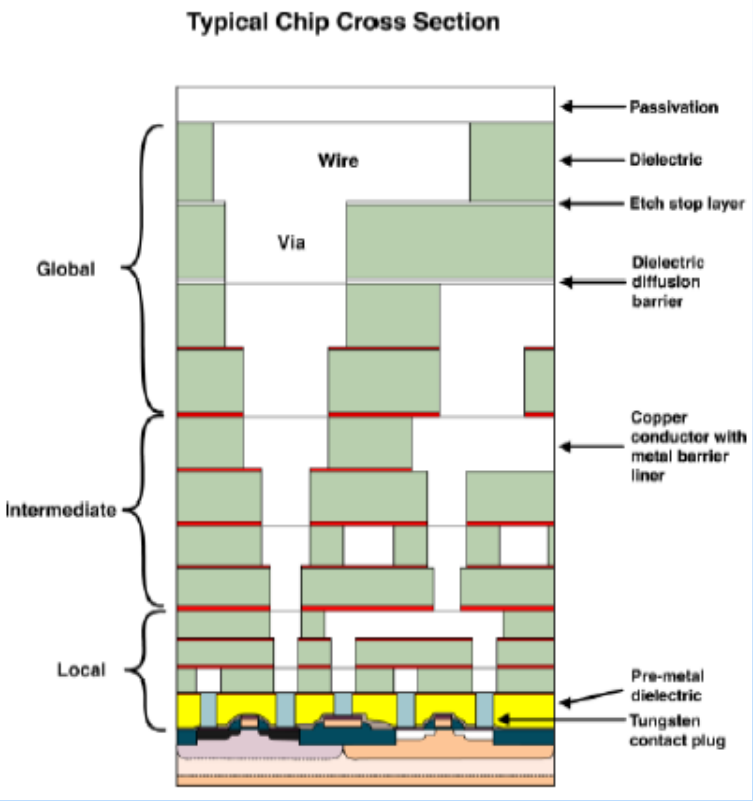
Michael J.Sampson
michael.j.sampson@nasa.gov
301-614-6233

Co- Managers NEPP Program

http://nepp.nasa.gov

NEPP Mission

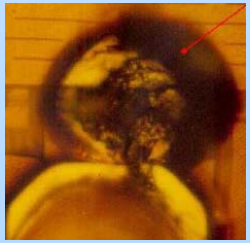
- **The NEPP mission is to provide guidance to NASA for the selection and application of microelectronics technologies, to improve understanding of the risks related to the use of these technologies in the space environment and to ensure that appropriate research is performed to meet NASA mission assurance needs.**



NEPP Overview

- **NEPP supports all of NASA for >20 years**
  - **7 NASA Centers and JPL actively participate**
- **The NEPP Program focuses on the reliability aspects of electronic devices**
  - **Three prime technical areas: *Parts (die), Packaging, and Radiation***
- **Alternately, reliability may be viewed as:**
  - **Lifetime, inherent failure and design issues related to the electronic parts technology and packaging,**
  - **Effects of space radiation and the space environment on these technologies, and**
  - **Creation and maintenance of the assurance support infrastructure required for mission success.**

Electrical overstress failure
in a commercial electronic device

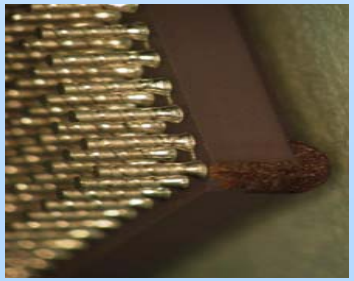


NEPP Works Two Sides of the Equation

- **Assurance**
  - ***Issues that are applicable to space systems being designed and built (i.e., currently available technologies)***
  - **Examples**
    - **Cracked capacitors**
    - **DC-DC converter reliability**
    - **Enhanced Low Dose Rate Sensitivity (ELDRS)**
  - **Communication infrastructure via website and working groups**
    - **NASA Electronic Parts Assurance Group (NEPAG)**
  - **Audit and review support**
- **New electronics technology**
  - ***Issues that are applicable to the next generation of space systems in conceptualization or preliminary design***
  - **Examples**
    - **45-90 nm CMOS**
    - **SiGe**
    - **State-of-the-art FPGAs**
  - **Collaboration with manufacturers and government programs for test, evaluation, and modeling**
  - **Development of new predictive performance tools**

NEPP Supports the Industry

- **NEPP has close, cooperative and long-standing relationships with government and non-government entities worldwide**
  - **Large university involvement**
  - **Close ties to many DoD/DOE agencies**
  - **International collaboration with JAXA, ESA, CNES, and others**
  - **Support for many working groups, organizations, and technical meetings including**
    - **G12, JEDEC, SPWG, IEEE NSREC and RADECS, IMAPS, SEE Symposium**
    - **NEPAG weekly telecons**
    - **Test and insertion guideline development**
- ***NEPP provides unique capabilities within NASA***
  - ***Evaluate technologies in advance of mission needs***
  - ***Provide assistance with risk management of technology insertion***

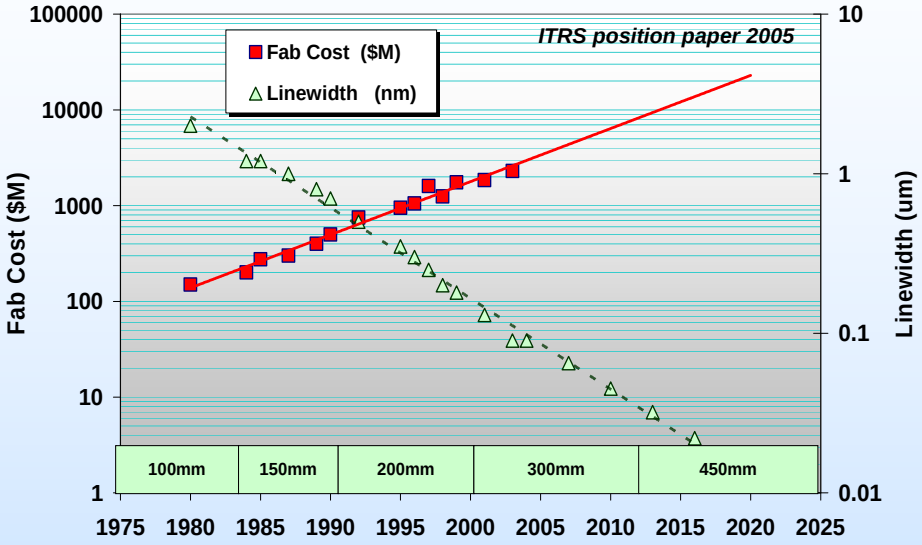


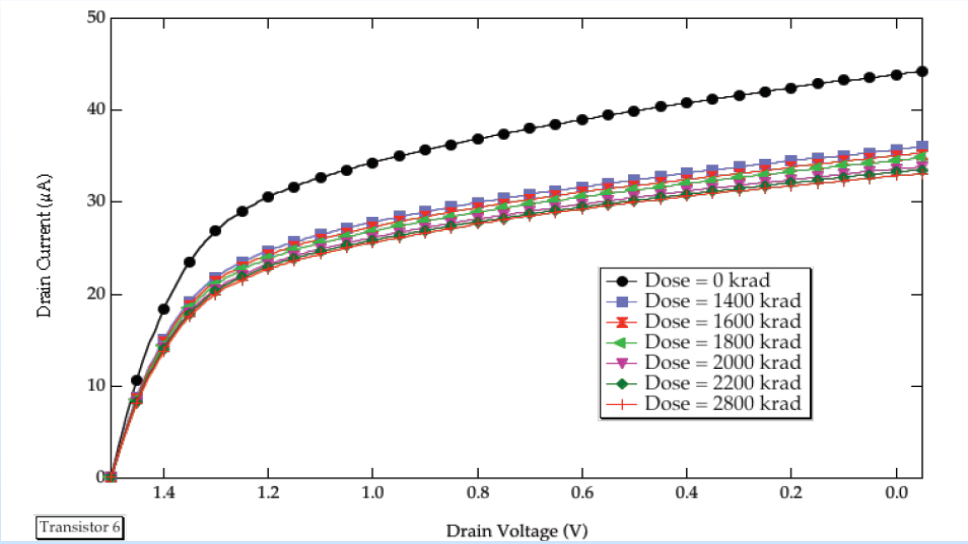
NEPP Has a Wide Range of FY09 Efforts

- **Tasks vary extensively in the technologies of interest**
  - **Building blocks like capacitors**
  - **Standard products like DC-DC Converters, linear bipolar devices, and A-to-D Converters**
  - **New commercial devices such as FPGAs and memories**
  - **Test structures on emerging commercial or radiation hardened technologies**
  - **Specialized electronics such as IR arrays and fiber optics**
  - **New assurance methods and investigations**
- **A few samples follow highlighting the work on radiation effects**

Many of the radiation tasks are in conjunction with DTRA

CMOS Scaling – New Challenges





Modeling, simulation, device physics understanding of failure modes, data gathering and analysis, and reliability prediction

- **Foundation for technology insertion of the next generation of scaled microelectronics.**

CMOS Scaling Reliability

NEPP POC: Mark White, JPL

Sample CMOS Scaling 90nm Transistor Test

CMOS Scaling Radiation

NEPP POC: Ken LaBel, GSFC

FY08/09 – CMOS Scaling and Radiation

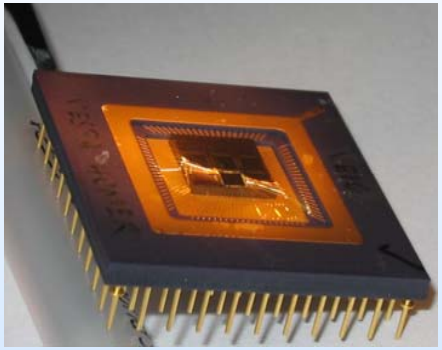
	90 nm	65 nm	45 nm	Notes
IBM		SOI and bulk SRAMs evaluated for SEE (proton and heavy ion)	SOI SRAMS received and test development begun	Collaboration with IBM and Sandia; Seeking structures for temporal SEE testing
Texas Instruments	TID on transistors completed (90 and 130 nm)	SEU/SEL on SRAMs completed; Awaiting transistors for TID	Discussing available SRAM test structures; Vanderbilt designing new test structures	Collaboration with TI and Vanderbilt; Experiments also performed at temperature
SIRF Program	TID on transistors completed	TID on transistors completed		Courtesy of Xilinx and AFRL; Experiments also performed with temperature
Intel		TID and dose rate completed	TID and dose rate planned on 1st commercially available Hi-K device *(Preliminary TID completed – functional only)*	Collaboration with Intel and NSWC

Additional discussions underway with eASIC and Freescale.

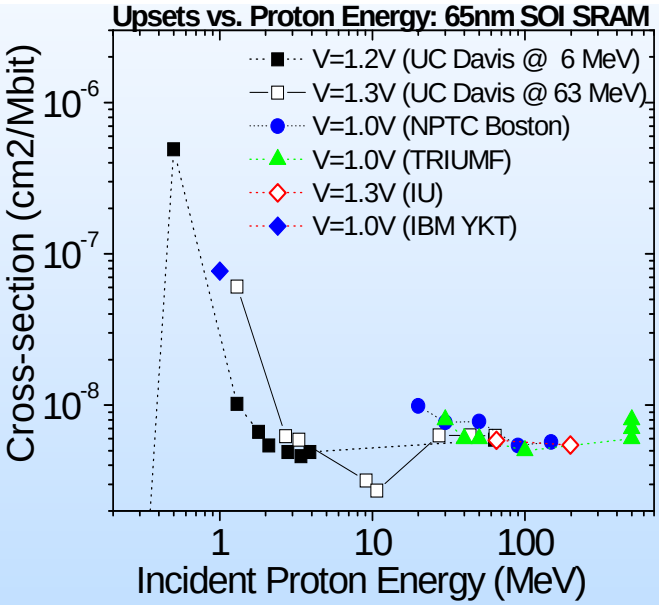
Support for RHBD efforts from DTRA/DARPA and AFRL

IBM 65nm SOI Results

Photo of 1Mbit 65nm SOI SRAM used for "front-side" testing



Data from 1 – 500 MeV @ normal incidence



Ratio of upsets from direct ionization vs. collision events

Shielding	SEU Ratio : Direct Ionization/Collision
50 mils	20 X
100 mils	10 X
200 mils	6 X
500 mils	3 X

MBU and angular analyses are still being performed.

Data taken from Heidel, et al, IEEE NSREC 2008

Intel Processors

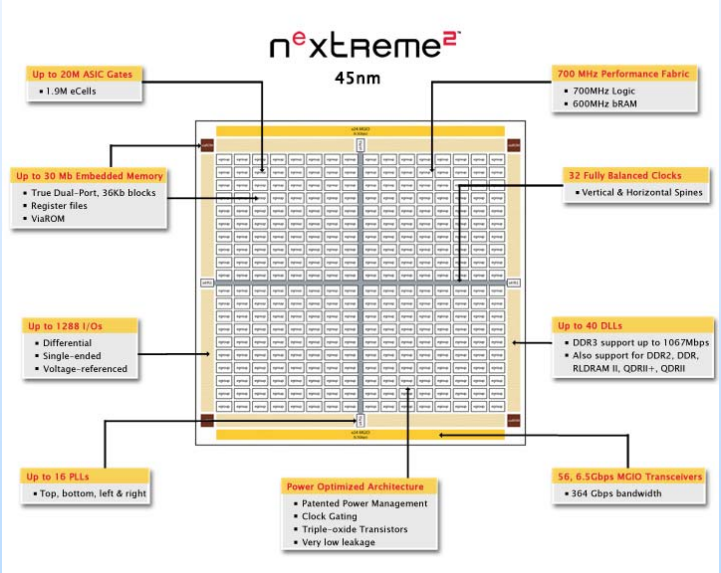
- **Efforts evaluating TID and dose rate on 65nm bulk CMOS processor were completed in FY08**
  - **Data may be requested via Intel**
- **45nm Wolfdale processor has been TID irradiated**
  - **Functional results show > 1 Mrad-Si tolerance**
  - **Results can NOT be inferred as exceeding ITAR levels without parametrics.**
  - **Full TID and dose rate planned**

3.0 Ghz, dual-core

First commercially available hi-K device

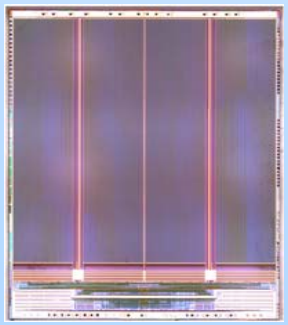
FPGAs and Related Devices

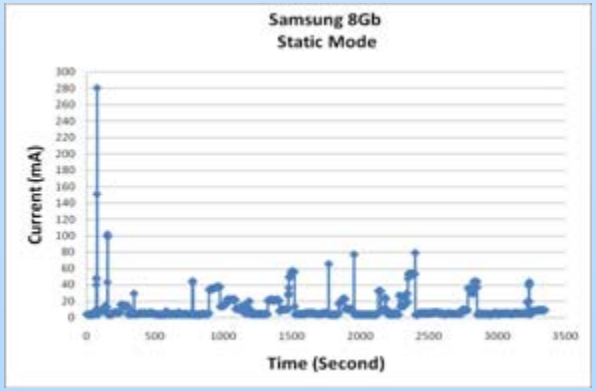
- FPGAs remain a "hot button" for NASA and much of the industry
  - Xilinx, ACTEL, Aeroflex, and Atmel, all have their insertions into NASA systems
- NEPP has continued to evaluate new technology devices via consortia (i.e., Xilinx Radiation Test Consortia) and independently
  - Support for the SIRF Program
  - Methodology for inter-comparison of FPGA SEU sensitivity for differing applications
  - System level considerations
- FY09 looks to continue and add
  - Further evaluation of peripheral devices (memory, power, IO)
  - Collaborations with Atmel on new 300 kgate FPGA
  - eASIC
    - New 45nm one mask programmable device



Flash Memories

- **Flash memories provide a huge advantage to space systems due to device density: 8 Mb monolithic devices are now available. Note: SDRAM efforts also exist under NEPP.**
- **Results in FY08 show promise for both SEU and TID**
  - **Testing looking at combined endurance and TID**
  - **SEU rates**
  - **Low dose rate exposures**
  - **Unbiased TID**
- **FY09 will continue with the state-of-the-art and investigate discrepancy in SEU results between GSFC and JPL on high current events**



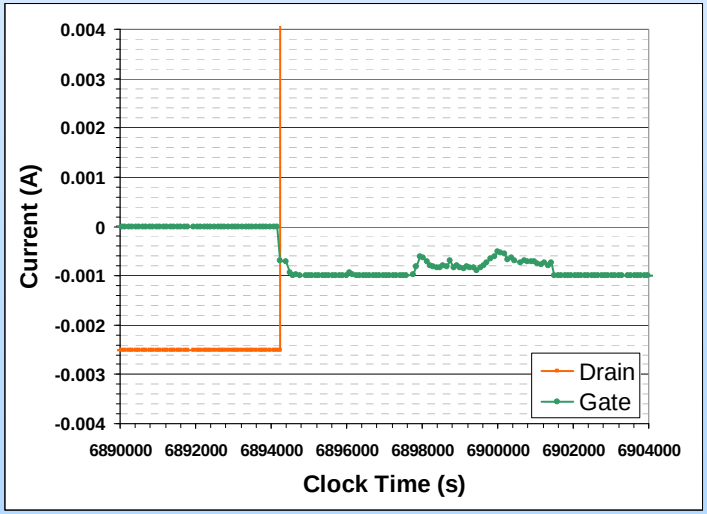


Power MOSFETs

- Power MOSFETs are critical in delivering power to both space systems and to science instrumentation
  - Applications run from a few V to > 1kV
- NEPP is developing updated guidance on test and safe operating areas (SOA) through test and modeling.
- Efforts include
  - Development of physics-based models for SEGR
  - Combined TID and SEE
    - Displacement damage?
  - Derating guidelines
  - Partial gate rupture/breaks

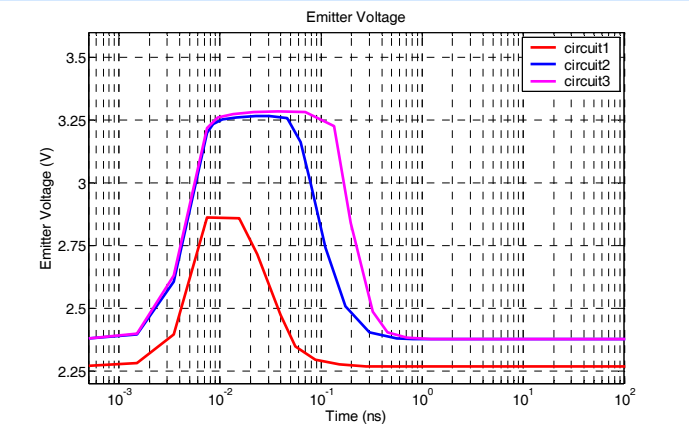
Table A2. Krypton; new device

Run #	DUT S/N	Fluence *ions/cm²*	Dose *rads (Si)*	Cumulative Dose *rads (Si)*	Vth *V*	BVdss *V*	Vgs *V*	Vds *V*	Pass/Fail
pretest	150	--	--	--	3.75	511	--	--	--
8	150	9.94E+04	45.86	45.86	3.32	511	0	200	Pass
9	150	1.03E+05	47.31	93.17	3.06	511	0	225	Pass
10	150	5.38E+04	24.8	117.97			0	250	Fail



Analog and Mixed Signal

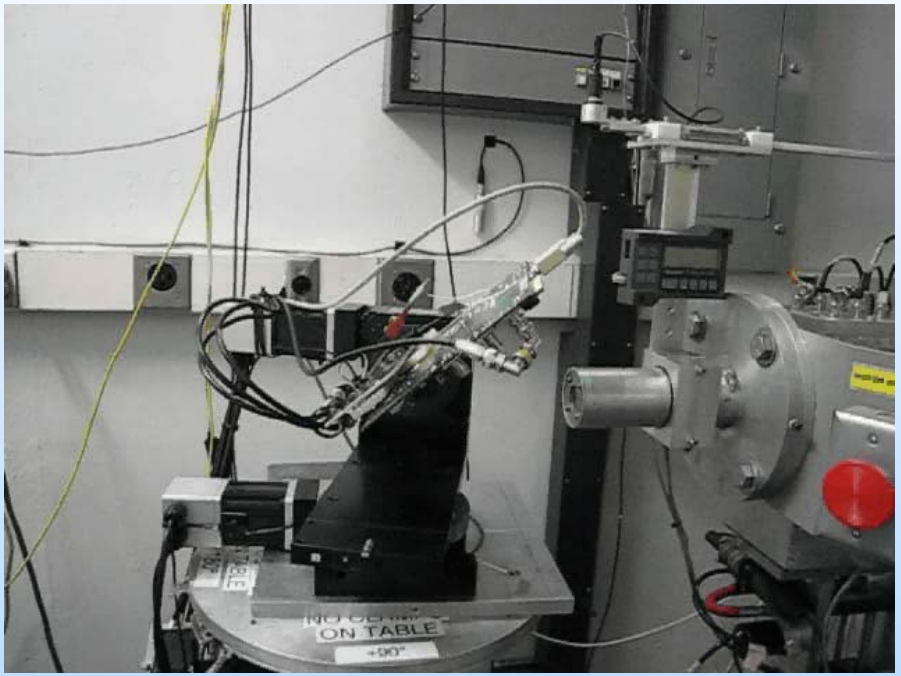
- SiGe
  - Test and modeling of SEU response
  - Damage testing
  - Charge collection model development
  - Cryo temp evaluation
  - Evaluation of RHBD on SiGe



- ELDRS at sub 10 mrad-Si
- Hydrogen effects on bipolars
- Advanced ADCs
  - Completed SEE testing on TI ADS5424 and NSC 14155 ADCs using new technique
  - Test guideline document under development
- Evaluation of LDOs, op amps and regulators
  - Working with NSC, LT, TI, and others

New Test Methods and Validation

- Conical SEE irradiation
  - Goniometer test system
- Dry ice storage (TID)
- TID performance at elevated temperature
- Combined TID and SEE performance
- Use of pulsed IV for transistor testing
- Laser testing of SDRAMs (w/NRL)
  - Establishment of test procedures
- Development of low proton energy SEU assurance
  - Test structures (SRAMs) and Xilinx FPGA



Summary

- The previous charts described some of the efforts supported by the NEPP Program
  - We have not described the Vanderbilt-led efforts for development of physics-based tools for SEU rate prediction, for example
- The NASA FY09 budget is still being developed (we are under continuing resolution), but the NEPP Program has undergone at least a 10% funding cut from our FY08 allocation
  - This will impact a number of efforts and reduce our ability to support universities and consortia
- If you are interested in collaboration or for more information, please feel free to contact us or visit the NEPP website at:

http://nepp.nasa.gov